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REMARKS

Applicant has amended claims 26-28 and 33-40. Attached hereto is a marked-up version showing the changes made to claims by the current amendment. Applicant respectfully requests that the Examiner consider and enter this amendment.

The amendment to the claims is supported in the application at least at page 3, lines 23-33; page 4, lines 6-25; and page 7, lines 7-31.

Claims 26-32 and 37-40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent number 5,313,101 (Harada et al.) in view of U.S. patent number 5,281,850 (Kanamori). Applicant respectfully traverses this rejection.

Claims 26-28, each as amended, define a semiconductor device with "a preformed titanium aluminide layer lining at least a bottom of [a] via hole." Claim 28, as amended, further defines the preformed titanium aluminide layer as "being volume reduced." Neither Harada et al. alone, nor in combination with Kanamori, teaches or suggests such a preformed titanium aluminide layer of a semiconductor device, much less that the layer is volume reduced.

Harada et al. discloses that (1) a titanium film (101) is deposited in a via hole (see column 9, specifically lines 41-46); (2) a titanium nitride film (102) is deposited over the titanium film (see column 9, lines 49-51); (3) an uppermost second aluminum interconnection layer (100) is deposited over the titanium nitride film (102) (see column 10, lines 19-23); and (4) a heat treatment is effected *after* depositing layer (100) for about 15-60 minutes at a temperature of 300°-450° C so as to promote mixing at the interface between the first and second aluminum interconnection layers (4) and (100), so that the intermetallic compound ($TiAl_3$) is formed by the heat treatment (column 10, lines 29-39). As described by Harada et al., the heat treatment is initiated *after* all the layers have been deposited (*i.e.,* the titanium layer, the titanium nitride layer, and the top aluminum layer) to convert the bottom titanium layer into the titanium aluminide compound referred to by

the Office Action in rejecting the claims (see column 10, lines 64-67). Clearly, the titanium aluminide layer in Harada et al. is not taught or suggested to be "preformed" as claimed, and further, there is absolutely no teaching or suggestion that the titanium aluminide layer is "volume reduced."

The Kanamori description cannot overcome the deficiencies of the Harada et al. reference. There is no teaching anywhere in Kanamori of any titanium aluminide layer, preformed or not. Thus, the subject matter of claims 26-28 is not rendered obvious by Harada et al. in view of Kanamori.

Because Harada et al., alone or in view of Kanamori, does not teach or suggest the preformed titanium aluminide layer, or that such a layer is volume reduced, these references do not render claims 26-28 unpatentable. Further, claims 29-32, depending from claim 28 are patentable for at least the same reason. Additionally, each depending claim, 29-32, is separately patentable because of its unique set of limitations. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 26-32 be withdrawn.

Claims 37-40, as amended, each define a computer system having a random access memory with "a preformed titanium aluminide layer lining at least a bottom of [a] via hole." Additionally, claims 39 and 40 further define the preformed titanium aluminide layer as "being volume reduced." For at least the reasons discussed above regarding claims 26-32, Harada et al., alone or in view of Kanamori, does not render claims 37-40 unpatentable. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 37-40 be withdrawn.

Claims 33-36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Harada et al. in view of Kanamori and further in view of Clayton. Applicant respectfully traverses this rejection.

Claims 33-36, as amended, each define a memory module having a random access memory with "a preformed titanium aluminide layer lining at least a bottom of [a]

via hole." Claims 35 and 36 further define the preformed titanium aluminide layer as "being volume reduced." For at least the reasons discussed above regarding claims 26-32, Harada et al., alone or in view of Kanamori, does not render claims 33-36 unpatentable.

Further, the Clayton description cannot overcome the deficiencies of the Harada et al. and Kanamori references. There is no teaching or suggestion anywhere in Clayton of any titanium aluminide layer, preformed or not.

The subject matter of claims 33-36 is not rendered obvious by Harada et al. in view of Kanamori and/or Clayton. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 37-40 be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to enter the amendment, withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By MJT #33,082

Mark J. Thronson
Registration No.: 33,082
Ryan H. Flax
Registration No.: 48,141
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 828-2232
Attorneys for Applicant

Version With Markings to Show Changes Made

26. (Twice Amended) A semiconductor device, comprising:

a metallic layer over a substrate;

an antireflective coating over said metallic layer;

a dielectric layer over said antireflective coating;

a via hole extending through the dielectric layer and said antireflective coating to a surface of the metallic layer;

a preformed titanium aluminide layer lining at least a bottom of the via hole; and

a conductive material formed on the titanium aluminide layer.

27. (Twice Amended) A semiconductor device, comprising:

an aluminum layer over a substrate;

a dielectric layer on the aluminum layer;

an antireflective coating over said dielectric layer;

a via hole extending through the dielectric layer and said antireflective coating to a surface of the aluminum layer;

a preformed titanium aluminide layer lining at least a bottom of the via hole;

a titanium nitride layer substantially free of through cracks formed on the titanium aluminide layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the plug material.

28. (Twice Amended) A semiconductor memory device, comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the substrate;

a second dielectric layer on the first metallic layer;

an antireflective coating over said second dielectric layer;

a via hole extending through the second dielectric layer and the antireflective coating to a surface of the second metallic layer;

a preformed titanium aluminide layer lining at least a bottom of the via hole, said preformed titanium aluminide layer being volume reduced;

a titanium compound layer formed on the titanium aluminide layer;

a conductive plug material on the titanium compound layer; and

a second metallic layer on the second dielectric layer and electrically connected to the plug material.

33. (Twice Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a first metallic layer over a substrate;

a dielectric layer on the first metallic layer;

an antireflective coating over the dielectric layer;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the first metallic layer;

a preformed titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer formed on the titanium aluminide layer;

a conductive plug material formed on the titanium compound layer; and

a second metallic layer on the dielectric layer and electrically connected to the plug material; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

34. (Twice Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a metallic layer over a substrate;

a dielectric layer on the metallic layer;

an antireflective coating over said dielectric layer;

a via hole extending through the dielectric layer and said antireflective coating to a surface of the metallic layer;

a preformed titanium aluminide layer lining at least a bottom of the via hole; and

a conductive material formed on the titanium aluminide layer; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

35. (Twice Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

an aluminum layer over a substrate;

a dielectric layer on the aluminum layer;

an antireflective coating over said dielectric layer;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the aluminum layer;

a preformed titanium aluminide layer lining at least a bottom of the via hole, said preformed titanium aluminide layer being volume reduced;

a titanium nitride layer substantially free of through cracks formed on the titanium aluminide layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the plug material; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

36. (Twice Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the substrate;

a second dielectric layer on the first metallic layer;

an antireflective coating over the second dielectric layer;

a via hole extending through the second dielectric layer and the antireflective coating to a surface of the second metallic layer;

a preformed titanium aluminide layer lining at least a bottom of the via hole, said preformed titanium aluminide layer being volume reduced;

a titanium compound layer formed on the titanium aluminide layer;

a conductive plug material on the titanium compound layer; and

a second metallic layer on the second dielectric layer and electrically connected to the plug material; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

37. (Twice Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a first metallic layer over a substrate;

a dielectric layer on the first metallic layer;

an antireflective coating over said dielectric layer;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the first metallic layer;

a preformed titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer formed on the titanium aluminide layer;

a conductive plug material formed on the titanium compound layer; and

a second metallic layer on the dielectric layer and electrically connected to the plug material.

38. (Twice Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a metallic layer over a substrate;

a dielectric layer on the metallic layer;

an antireflective coating over the dielectric layer;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the metallic layer;

a preformed titanium aluminide [liner] layer lining at least a bottom of the via hole; and

a conductive material formed on the titanium aluminide liner.

39. (Twice Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

an aluminum layer over a substrate;

a dielectric layer on the aluminum layer;

an antireflective coating over the dielectric layer;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the aluminum layer;

a preformed titanium aluminide layer lining at least a bottom of the via hole, said preformed titanium aluminide layer being volume reduced;

a titanium nitride layer substantially free of through cracks formed on the titanium aluminide layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the plug material.

40. (Twice Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the substrate;

a second dielectric layer on the first metallic layer;

an antireflective coating over the second dielectric layer;

a via hole extending through the second dielectric layer and the antireflective coating to a surface of the second metallic layer;

a preformed titanium aluminide layer lining at least a bottom of the via hole, said preformed titanium aluminide layer being volume reduced;

a titanium compound layer formed on the titanium aluminide layer;

a conductive plug material on the titanium compound layer; and

a second metallic layer on the second dielectric layer and electrically connected to the plug material.